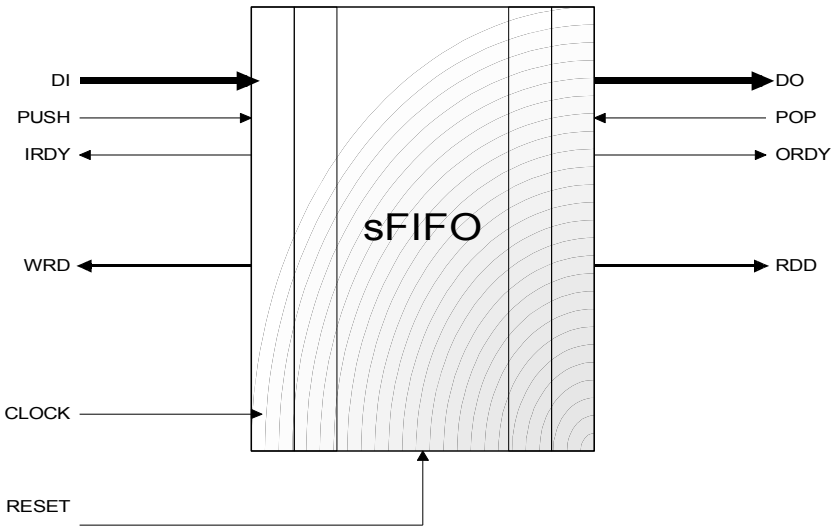
A2sFIFO
Synchronous FIFO



sFIFO Symbol

FEATURES

- Fully Synthesizable RTL - Verilog
- Static Timing Analysis compatible
- Dual-port inferred RAM architecture
- Configurable width, depth & fallthrough
- Standard FIFO handshake interface
- Flags or depth values on each port

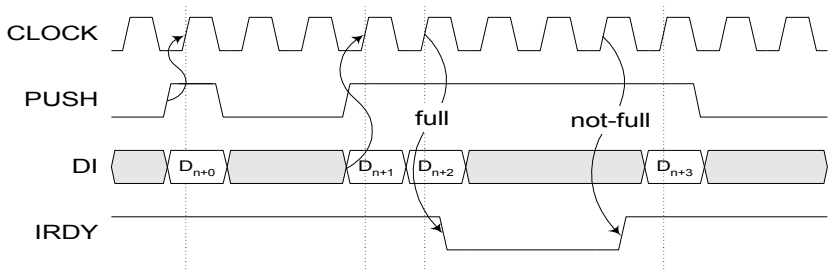
APPLICATIONS

- Fully Synchronous buffering in a single clock domain

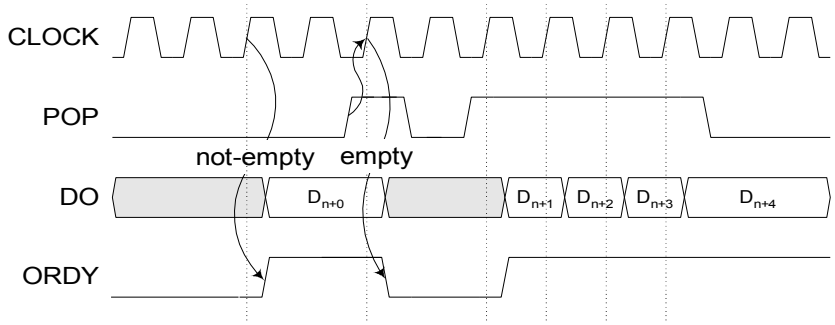
The sFIFO controls are designed to operate over a wide range of clock frequencies. The interface signals are fully synchronous; no asynchronous signals are present on either side. Only reset may be asynchronous in that it may be asserted asynchronously and synchronized internally to the clock.

The FIFO also has a programmable fall-through for first data entering an empty FIFO. It may be “0” in which case the input is passed combinatorially to the output, or “1” where the FIFO appears like a simple register.

Signal Name	Width	I/O	Description
Write Interface			
DI	Parameter	In	Data In
PUSH	1	In	Push Data Input the FIFO on next WR-CLOCK edge (rising or falling set by parameter)
IRDY	1	Out	Input Ready. FIFO is NOT full and can accept incoming data
WRD	Parameter	Out	Write Depth. Either a depth value or a parameter set depth threshold flag
Read Interface			
DO	Parameter	Out	Data Out
POP	1	In	Pop Data Output from the FIFO on next RD-CLOCK edge (rising or falling set by parameter)
ORDY	1	Out	Output Ready. FIFO is NOT empty and is presenting data to be read
RDD	Parameter	Out	Read Depth. Either a depth value or a parameter set depth threshold flag
System Interface			
RESET	1	In	Reset. Asynchronous Active, Synchronous Inactive
CLOCK	1	In	System Clock



sFIFO Write Interface Timing



sFIFO Read Interface Timing