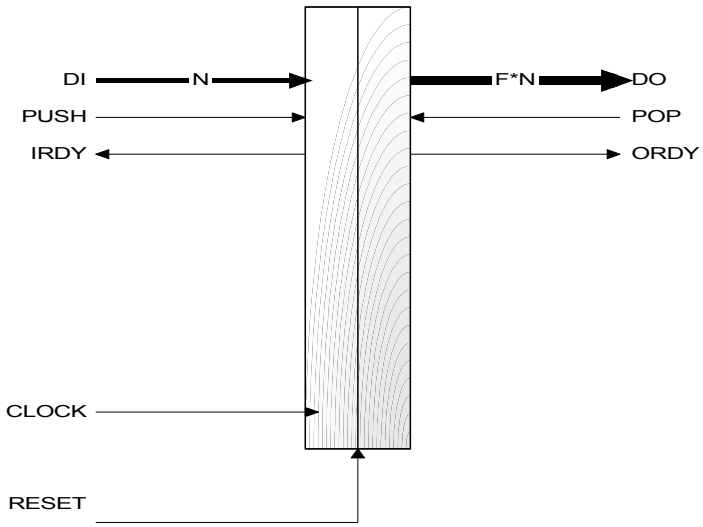
Advanced Architectures

A2 PIPE

Stallable 1-to-N expansion PIPESTAGE



PIPE Symbol

FEATURES

- Fully Synthesizable RTL - Verilog
- Parameterized Expansion Factor
- Static Timing Analysis compatible
- Double Register for synchronous pipeline
- Configurable width
- Standard FIFO handshake interface

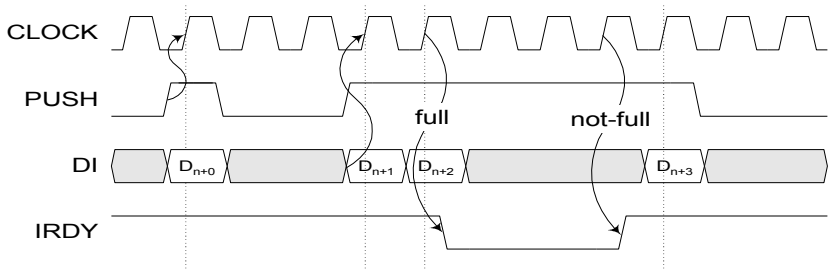
APPLICATIONS

- Fully Synchronous pipelines
- Width Expansion

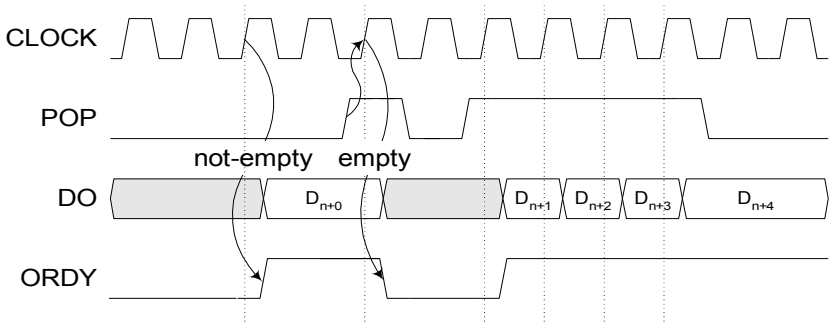
The PIPE is a double register plus a small state machine that enables a fully synchronous stall-able pipeline to be built. A parameter defines the ratio of the input width to the output width. For example, if the input width is 8-bits and the Expansion Factor is 4 the the output width is 32-bits. The ORDY ready signal will indicate when at least a whole output word is available. The interface is fully compatible with a Standard FIFO interface and they may be mixed and matched. A “Stall” may be generated by gating the POP and ORDY signals to arrest the normal flow of data down the pipeline and allows any given stage to take multiple cycles when necessary. In doing so the IRDY signal is removed in the following cycle and the data that was to replace the data in the primary register is saved into the secondary register. When the “Stall” is removed the the secondary register

contents are copied to the primary register and the IRDY is re-asserted for the next clock edge.

Signal Name	Width	I/O	Description
Write Interface			
DI	Parameter	In	Data In
PUSH	1	In	Push Data Input the FIFO on next WR-CLOCK edge (rising or falling set by parameter)
IRDY	1	Out	Input Ready. FIFO is NOT full and can accept incoming data
Read Interface			
DO	Parameter	Out	Data Out
POP	1	In	Pop Data Output from the FIFO on next RD-CLOCK edge (rising or falling set by parameter)
ORDY	1	Out	Output Ready. FIFO is NOT empty and is presenting data to be read
System Interface			
RESET	1	In	Reset. Asynchronous Active, Synchronous Inactive
CLOCK	1	In	System Clock



PIPE Write Interface Timing



PIPE Read Interface Timing