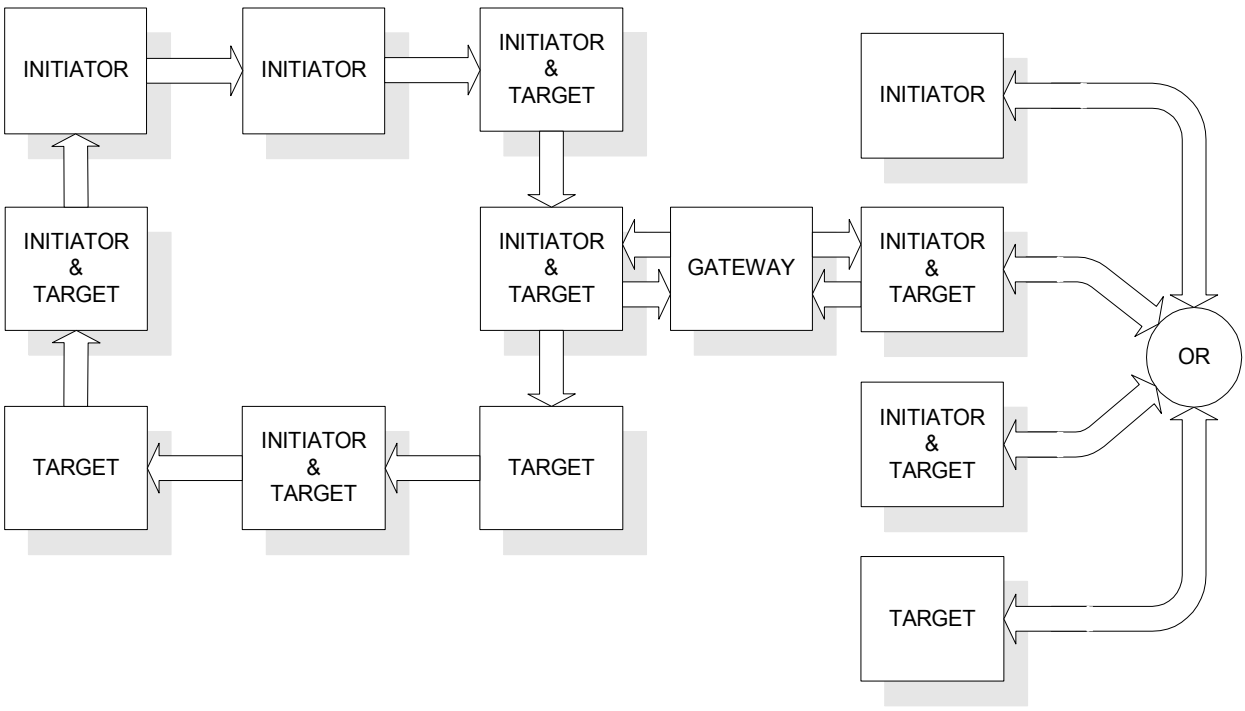
Advanced Architectures

A2R Control Interconnect



FEATURES

- **DATA PATHS**
  Multiplexed Address and Data for minimum physical interconnect.
  32-bit or 64-bit width
- **ADDRESSING**
  Customizable assignment of address space
  A2P debug compatible (Host Interface)
- **ARBITRATION**
  User-configurable / customizable
  Multi-level
- **BRIDGES**
  Gateways between segments
  Segements may operate independently
- **EXTENSIONS**
  Parity or ECC protection on all paths
  Multi-processing support
  User defined fields
  Alert broadcasting (interrupts)
- **PROTOCOLS**
  Simple Initiator & Target interfaces
  Multiple initiator and target
  Focused on register reads and writes
- **DEVICES**
  Any number of transaction initiators
  Any number of transaction targets
- **FABRIC**
  Point-to-point token ring
  Pipelined point-to-point
  Parallel OR gate
- **INTERFACES**
  Veneers to other protocols (OCP, AMBA..)

OVERVIEW

A2R provides an interconnection mechanism between control registers in an ASIC design and any number of control devices; CPUs, debug ports etc.. The bus is especially suited for synthesizable designs. It is specifically developed to meet the challenges of long interconnect delays in large System-on-chip designs and can be tailored to match system clock rates.

A2R is a fully synchronous auxiliary bus that is user configurable to provide a wide variety of performances to best match the system level requirements of a particular implementation. The user (system architect) can configure the system for address and data widths, may add special bus fields to transfer custom information and may select the arbitration algorithm. Bridges (called Gateways) can also be included to allow different bus sections to operate independently. In order to access through the gate an initiator signals the gateway to request the upper level bus and send its access upwards. This mechanism allows the initiators in separate segments to access within their segment at any time and only at a higher level through a higher-level arbitration.

Local interconnections between sub-modules are often configured using an OR structure as the A2R fabric and inter-module connections are configured to use a ring structure. This point-to-point topology can then be pipelined so that all sections of the ring settle within a single clock cycle this allows the A2R to be configured such that only single cycle operations exist and no false path or multi-cycle paths exist which significantly eases timing closure in large SoC designs.